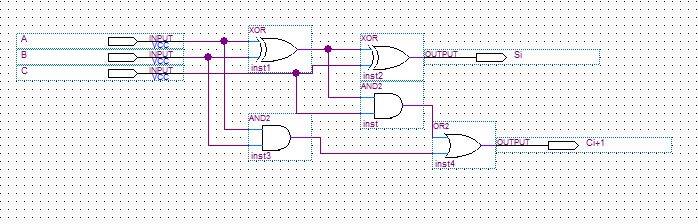
**Objectives:**

1. To implement and test a full adder using random gates.

2. To implement and test a 4-bit 2’s complement adder/subtractor using IC 7483 (4-bit binary adder).

**Answer to the Pre-Lab Question:**

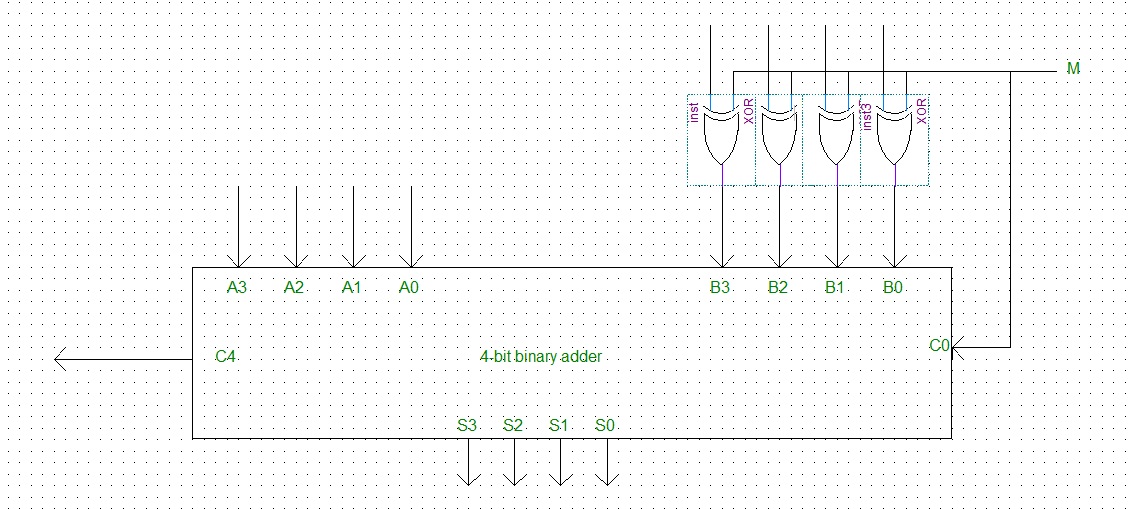
1.



2.

|  |  |
| --- | --- |
| A B C | C S |
| 0 0 0 | 0 0 |
| 0 0 1 | 0 1 |
| 0 1 0 | 0 1 |
| 0 1 1 | 1 0 |
| 1 0 0 | 0 1 |
| 1 0 1 | 1 0 |
| 1 1 0 | 1 0 |
| 1 1 1 | 1 1 |

3.



4.

|  |  |
| --- | --- |
| 3+3    3 = 0011  3 = 0011  0110  = +6 | 3-2    3 = 0011  -2 = 1110  10001  = +1 |
| 3+4    3 = 0011  4 = 0100  0111  = +7 | 3-3    3 = 0011  -3 = 1101  00000  = 0 |
| 3+5    3 = 0011  5 = 0101  1000  = +8 | 3-4    3 = 0011  -4 = 1100  1111  = -1 |

**EAST WEST UNIVERSITY**

**Semester:** Fall 2016

**Course Number:** CSE 345

**Course Title:** Digital Logic Design

**Experiment No:** 04

**Experiment Title:** Binary adder and subtractor

**Name:** Md. Sakibur Rahman

**ID:** 2014-1-60-032

**Group Number:** 02

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**Date of Performance:** November 02, 2016